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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	4294US (98-1208)
First Inventor or Application Identifier	John Whitman
Title	SPIN COATING FOR MAXIMUM FILL CHARACTERISTIC YIELDING A PLANARIZED THIN FILM SURFACE
Express Mail Label No.	EL500248224US

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APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification [Total Pages 37] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 5]
4. Oath or Declaration [Total Pages 2]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 5 below]***
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
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ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [X] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
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17. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No. _____/_____

Prior application information: Examiner _____ Group / Art Unit: _____

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APPLICATION FOR LETTERS PATENT

for

SPIN COATING FOR MAXIMUM FILL CHARACTERISTIC YIELDING A PLANARIZED THIN FILM SURFACE

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SPIN COATING FOR MAXIMUM FILL CHARACTERISTIC YIELDING A PLANARIZED THIN FILM SURFACE

BACKGROUND OF THE INVENTION

Field of the Invention: The present invention relates to methods for filling containers, trenches, or other recesses of semiconductor devices structures during fabrication thereof. Particularly, the present invention relates to the use of spin coating techniques to fill containers, trenches, and other recesses of semiconductor device structures. As a specific example, the present invention relates to a method for masking hemispherical grain (HSG) silicon-lined containers of a stacked capacitor structure to facilitate removal of HSG silicon from the surface of a semiconductor device structure including the stacked capacitor structure.

Background of Related Art: Conventionally, spin-on processes have been used to apply substantially planar layers of material to the surfaces of semiconductor device structures being fabricated upon a wafer of semiconductor material (e.g., a silicon, gallium arsenide, or indium phosphide wafer) or other semiconductor substrate (e.g., a silicon on insulator (SOI), silicon on glass (SOG) silicon on ceramic (SOC), silicon on sapphire (SOS), or other similar substrate). Consequently, while the portions of a spun-on layer of material over substantially horizontal structures may be substantially planar, the layer of material may not substantially fill or conform to the numerous, minute recesses formed in the semiconductor device structure.

For example, when it is desirable to mask a container, trench, or other recess of a semiconductor device structure without masking the surface of the semiconductor device structure to which the container, trench, or other recess opens, a mask material is typically applied to the surface of the semiconductor device structure, such as by use of known spin-on processes. As an example, FIG. 1 illustrates the fabrication of a stacked capacitor structure 10 with conductively doped HSG silicon 16-lined containers 14. As it is necessary to remove HSG silicon 16 from a surface 12 of an electrical insulator layer 11 (e.g., borophosphosilicate glass (BPSG), phosphosilicate glass (PSG), or borosilicate glass (BSG)) of stacked capacitor structure 10 to prevent electrical shorting between

adjacent containers 14, mask material 18′ is introduced into containers 14 to facilitate removal of HSG silicon 16 from surface 12.

While conventional spin-on processes will force some of the mask material into containers 14, trenches, or other recesses, these processes typically result in the formation of a relatively thick, but not necessarily planar layer of mask material 18′ over surface 12. Due to various factors, including the surface tension of mask material 18′ and the centrifugal forces applied to mask material 18′ during the spin-on process, mask material 18′ tends to migrate out of the small recesses (e.g., containers 14) formed in surface 12. Thus, the thickness of mask material 18′ within a container 14, trench, or other recess may not be significantly greater than the thickness of mask material 18′ covering surface 12, leaving containers 14 partially unfilled. Once the layer of material has been dispensed onto the semiconductor device structure, it is solidified or cured, such as by known photographic or soft bake processes.

In order to reduce the thickness of the layer of mask material covering the surface of the semiconductor device structure without substantially decreasing the thickness of the layer of mask material within the recesses, chemical-mechanical planarization (CMP) processes, such as chemical-mechanical polishing techniques, are typically employed. The use of CMP processes is, however, somewhat undesirable since such processes are known to create defects in the surface of the semiconductor device structure. CMP processes are also known to leave debris, or contaminants, which may be trapped in defects in the surface of the semiconductor device structure and which may subsequently cause electrical shorting of a fabricated semiconductor device. For example, if CMP processes are used to remove mask material and at least part of a conductively doped HSG silicon layer from an insulator at the surface of a stacked capacitor structure, conductive silicon particles may be trapped in defects in the surface of the insulator and subsequently cause electrical shorting between adjacent containers of the stacked capacitor. These potentially damaging contaminants may remain even when a chemical removal process, such as a wet or dry etch, follows the CMP process.

Alternatively, a photoresist may be used as the mask material. Patterning of the photoresist requires several steps in which equipment must be precisely aligned with features, such as the containers of a stacked capacitor structure, fabricated on the semiconductor substrate. Additional handling of the semiconductor device structure is also required when a photoresist is used to mask containers, trenches, or other recesses formed in a semiconductor device structure, which is somewhat undesirable.

Moreover, when conventional blanket deposition techniques are used to fill the recesses of a semiconductor device structure with a material (e.g., to fill the trenches of a shallow trench isolation structure with an electrical insulator material and to fill dual damascene trenches with a conductive material), the material typically forms a nonplanar layer over the semiconductor device structure. Such material layers typically include valleys located over recesses in the underlying semiconductor device structure and peaks located over other regions of the semiconductor device structure. Chemical-mechanical planarization is an example of a conventional technique for removing such materials from the surface of a semiconductor device structure while leaving these materials within the recesses of the semiconductor device structure. As chemical-mechanical planarization processes typically employ an abrasive pad to mechanically planarize structures, however, the peaks of the material layer may break off in larger than desired pieces and subsequently scratch the surface of the semiconductor device structure, forming defects therein.

The art does not teach a semiconductor device structure that includes a non-chemical-mechanical planarized material layer that substantially fills a container, trench, or other recess formed in the semiconductor device structure and which does not substantially cover the remainder of a surface of the semiconductor device structure or which includes only a relatively thin layer of material over the remainder of the surface. The art also fails to teach a method for forming a material layer with these features. In addition, the art lacks teaching of a method for reducing the likelihood that peaks of a nonplanar layer of material will damage a surface of a semiconductor device structure during subsequent planarization of the layer of material.

SUMMARY OF THE INVENTION

The present invention includes semiconductor device structures with substantially planar surfaces. The semiconductor device structures also include containers, trenches, or other recesses that are filled with a material. The material may also cover adjacent, surfaces of the semiconductor structures. If the material covers surfaces of the semiconductor device structures, the thickness of the material covering the surface is less than the depth of the containers, trenches, or other recesses that are substantially filled with material. Preferably, the thicknesses of material covering the surfaces of the semiconductor device structures are less than about half the depth of the containers, trenches, or other recesses. The surfaces of the material or materials that fill the recesses and that may cover the surfaces of the semiconductor device structures have not, however, been chemical-mechanical planarized to achieve the reduced depth of material outside of the recesses.

In one embodiment of the present invention, the semiconductor device structure includes a stacked capacitor structure with a layer of electrically insulative material, or insulator layer, and at least one container recessed or formed in the insulator layer. The insulator layer includes a substantially planar surface, which is referred to herein as the exposed surface of the insulator layer. A layer of electrically conductive material covers the surface of the insulator layer and lines the at least one container. By way of example, the electrically conductive material may be conductively doped hemispherical grain (HSG) silicon. As the stacked capacitor structure would electrically short if the conductive material remained on the surface of the insulator layer between adjacent containers, for the stacked capacitor to function properly the conductive material must be removed from the surface of the insulator layer prior to completing fabrication of the stacked capacitor, but remain within the containers. Thus, this embodiment of the semiconductor device structure includes a substantially planar surface with a non-chemical-mechanical planarized quantity of mask material substantially filling the at least one container. While the mask material may cover regions of the layer of conductive material overlying the surface of the insulator layer, it is preferred that these regions are substantially uncovered by mask material. If mask material does overly these regions of

the layer of conductive material, the thickness of the mask material overlying these regions is less than the depth of the at least one container. Preferably, the thickness of the mask material over these regions of the layer of conductive material is less than about half the depth of the at least one container.

The mask material may be applied to the semiconductor device structure by known processes and is spread across the surface of the stacked capacitor structure so as to substantially fill the at least one container while leaving a thinner, or no, material layer over regions of the layer of conductive material that overly the surface of the insulator layer. For example, the mask material may be spread across the surface of the stacked capacitor structure by use of spin-on techniques, wherein the mask material is applied at a first speed, the rate of spinning is decreased to a second speed at which the mask material is permitted to at least partially set up, then the rate of spinning is gradually increased, or ramped up, to a third speed at which a desired, reduced thickness of mask material covering the surface may be obtained. The rate at which the stacked capacitor structure is spun may again be decreased to permit the mask material to further set. An edge bead of mask material may then be removed from the stacked capacitor structure and the stacked capacitor structure spun once again to remove solvents from the mask material.

In another embodiment of the semiconductor device structure, a mask is disposed over a shallow trench isolation (STI) structure that includes a semiconductor substrate with a substantially planar surface and shallow trenches recessed, or formed, in the semiconductor substrate. The semiconductor device structure has a substantially planar surface, without requiring chemical-mechanical planarization of the surface of the mask. If material of the mask covers the surface of the semiconductor substrate, the thickness of mask material thereover is significantly less than the depths of the shallow trenches. Preferably, the thickness of mask material covering the surface of the semiconductor substrate is less than about half the depths of the trenches. More preferably, the surface of the semiconductor substrate remains substantially uncovered by the mask material. The present embodiment of the semiconductor substrate may also include conductively doped regions continuous with the surface and located between the trenches formed in the semiconductor substrate.

The shallow trench isolation structure may be formed by known processes. The mask may be formed by applying a quantity of mask material to the shallow trench isolation structure and spreading the mask material over the surface of the shallow trench isolation structure so as to substantially fill each trench thereof. As an example of the manner in which mask material may be spread across the shallow trench isolation structure, the mask material may be spun across the semiconductor substrate at a first speed, the rate of spinning decreased to a second speed to permit the mask material to at least partially set up while remaining in the trenches, then the rate of spinning gradually increased, or ramped up, to a third speed at which a desired, reduced thickness of mask material covering the surface may be obtained. The rate at which the shallow trench isolation structure is spun may again be decreased to permit the mask material to further set. An edge bead of mask material may then be removed from the shallow trench isolation structure and the shallow trench isolation structure spun once again to remove solvents from the mask material. Conductively doped regions of the semiconductor substrate may be formed by exposing the substrate and mask material to a conductivity dopant. The regions of the semiconductor substrate that remain uncovered or that are covered with thinner layers of the mask material (e.g., the surface of the semiconductor substrate) are implanted with the conductivity dopant while regions of the semiconductor substrate that are covered with thicker layers of the mask material (e.g., regions of the semiconductor substrate beneath the trenches) remain substantially undoped.

Another embodiment of a semiconductor device structure according to the present invention includes a surface with one or more recesses formed therein and a layer of a first material substantially filling each recess and at least partially covering the surface. The layer of first material has a nonplanar surface and may include a valley located substantially over each recess in the semiconductor device structure and one or more peaks located substantially over the surface of the semiconductor device structure. A second material disposed over the layer of first material at least partially fills each of the valleys formed in the layer of first material. The second material has a substantially planar surface that is not further planarized following formation thereof.

By way of example, the semiconductor device structure may be a shallow trench isolation structure including a semiconductor substrate with a substantially planar surface and trenches recessed, or formed, in the semiconductor substrate. The trenches are filled with a first, electrically insulative material, which is preferably a low dielectric constant, or "low-k", material, such as a high density plasma (HDP) silicon oxide, or HDP oxide. HDP oxide or another insulative material may be disposed into the trenches by way of known processes, such as chemical vapor deposition (CVD) processes. As the processes that are used to fill the shallow trenches with the first, insulative material are typically blanket deposition processes, the insulative material may also cover the surface of the semiconductor substrate. The surface of a layer of the first, insulative material blanket deposited over a semiconductor substrate with trenches formed therein is nonplanar.

As another example of the deposition of a first material over a semiconductor device structure, each recess of the semiconductor device structure may be a dual damascene type trench substantially filled with a first, conductive material. The first, conductive material may be disposed into each dual damascene trench of the semiconductor device structure by known processes, such as physical vapor deposition (PVD) (e.g., sputtering) or chemical vapor deposition techniques. Since these processes typically form a layer of material that blankets substantially the entire semiconductor device structure, the first, conductive material may also cover the surface of the semiconductor device structure. When blanket deposited over a semiconductor device structure with trenches formed therein, such layers typically have nonplanar surfaces.

The second material is preferably a stress buffer material that facilitates planarization of the layer of insulative material without causing substantial defects in either the insulative material or in the surface of the underlying semiconductor substrate. Exemplary materials that are useful as the stress buffer include resins and polymers that may be applied by way of spin-on techniques. The stress buffer has a substantially planar surface and preferably fills the valleys in the layer of insulative material without substantially covering the peaks thereof.

After the stress buffer material is applied to the semiconductor device structure, it may be spread across the surface of the semiconductor device by a spin-on technique that

includes spinning the semiconductor device structure at a first speed, decreasing the rate of spinning to a second speed at which the material of the stress buffer within the valleys is permitted to at least partially set, then gradually increasing, or ramping up the rate of spinning to a third speed at which a desired thickness of stress buffer material covering the surface may be obtained. The rate at which the semiconductor device structure stacked is spun may again be decreased to permit the stress buffer material to further set. An edge bead of stress buffer material may then be removed from the semiconductor device structure and the semiconductor device structure spun once again to remove solvents from the stress buffer material.

If portions of the first material layer protrude through the second material, all or part of the first material layer may removed with selectivity over the second material by known processes, such as by use of wet or dry etchants. The protruding portions of the first material layer may be partially removed until a surface of the first material is in substantially the same plane as a surface of the second material. The first and second materials may then be substantially concurrently removed from over the surface of the semiconductor device structure by known chemical-mechanical planarization or etching processes. Following the removal of the first and second materials, the surface of first material remaining in each recess is preferably substantially flush with the surface of the semiconductor device structure. Alternatively, the first material can be selectively removed to expose the surface of the semiconductor device structure, then the second material removed therefrom.

If the semiconductor device structure has a substantially planar surface after the second material is disposed thereon, the first and second materials may be substantially concurrently removed by known chemical-mechanical planarization or etching processes to provide a semiconductor device structure with first material substantially filling the recesses thereof and having a substantially planar surface.

Other features and advantages of the present invention will become apparent to those of skill in the art through consideration of the ensuing description, the accompanying drawings, and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 (Prior Art) is a cross-sectional representation of stacked capacitor structure with a surface and containers lined with conductively doped hemispherical grain polysilicon and including a conventionally spun-on layer of mask material thereover;

FIG. 2 is a cross-sectional representation of a stacked capacitor structure including a layer of mask material substantially filling the containers thereof and having a substantially planar surface;

FIG. 3 is a cross-sectional representation of the stacked capacitor structure of FIG. 2, depicting the mask material and conductively doped hemispherical grain polysilicon removed from over the surface, the containers remaining substantially filled with mask material;

FIG. 4 is a cross-sectional representation of the stacked capacitor structure of FIG. 3 with the mask material removed from the containers;

FIG. 5 is a cross-sectional representation of a shallow trench isolation structure including a semiconductor substrate with a surface and trenches formed in the surface and a layer of mask material that substantially fills the trenches and has a substantially planar surface;

FIG. 6 is a cross-sectional representation of the shallow trench isolation structure of FIG. 5 that schematically illustrates doping of portions of the semiconductor substrate that are continuous with the surface and laterally adjacent the trenches without doping of portions of the semiconductor substrate beneath the trenches;

FIG. 7 is a cross-sectional representation of a shallow trench isolation structure including a nonplanar layer of electrically nonconductive material filling the trenches and overlying the surface thereof and a layer of stress buffer material with a substantially planar surface filling recesses in and overlying the layer of electrically nonconductive material;

FIG. 8 is a cross-sectional representation of a variation of the shallow trench isolation structure of FIG. 7, which includes stress buffer material with a substantially planar surface partially filling recesses in the layer of electrically nonconductive material;

FIG. 9 is a cross-sectional representation of the shallow trench isolation structure of FIG. 8, depicting the layer of electrically nonconductive material partially removed to form a substantially planar surface flush with the surfaces of the stress buffer material in the recesses of the layer;

FIG. 10 is a cross-sectional representation of the shallow trench isolation structure of FIG. 9, illustrating stress buffer material disposed at least partially over the electrically nonconductive material remaining in the trenches;

FIG. 11 is a cross-sectional representation of the shallow trench isolation structures of FIGs. 7 and 10, depicting the electrically nonconductive material within the trenches as having a substantially planar surface that is substantially flush with the surfaces of the semiconductor substrate of the shallow trench isolation structures;

FIG. 12 is a cross-sectional representation of a semiconductor device structure including dual damascene trenches recessed in a surface thereof, a nonplanar layer of conductive material substantially filling the trenches and covering the surface of the semiconductor device structure, and a layer of stress buffer material with a substantially planar surface disposed over and filling recesses in over the layer of conductive material;

FIG. 13 is a cross-sectional representation of a variation of the semiconductor device structure of FIG. 12, which includes stress buffer material with a substantially planar surface only partially filling recesses formed in the layer of conductive material;

FIG. 14 is a cross-sectional representation of the semiconductor device structure of FIG. 13, depicting the layer of conductive material partially removed to form a substantially planar surface flush with the surfaces of the stress buffer material in the recesses of the layer;

FIG. 15 is a cross-sectional representation of the semiconductor device structure of FIG. 14, illustrating stress buffer material partially disposed at least partially over the conductive material remaining in the trenches; and

FIG. 16 is a cross-sectional representation of the semiconductor structures of FIGs. 12 and 15, depicting the conductive material within the trenches as having a substantially planar surface that is substantially flush with the surfaces of the semiconductor device structures.

DETAILED DESCRIPTION OF THE INVENTION

With reference to FIG. 2, a semiconductor device structure, in this case a stacked capacitor structure 10 incorporating teachings of the present invention is illustrated. Stacked capacitor structure 10 includes a surface 12 with containers 14 recessed, or formed, in surface 12. As illustrated, surface 12 and containers 14 are lined with a layer 16 of conductively doped hemispherical grain silicon. Stacked capacitor structure 10 also includes a mask layer 18 of a polymer material (e.g., polyimide or photoresist) disposed over layer 16. Mask layer 18 substantially fills containers 14 and has a substantially planar exposed surface 19. The thickness T of portions of mask layer 18 overlying surface 12 is less than the depth D of containers 14 and, preferably, is less than about half of depth D.

Stacked capacitor structure 10, including the conductively doped hemispherical grain silicon layer 16 thereof, may be fabricated by known processes, such as those disclosed in U.S. Patent 5,663,090, issued to Dennison et al. on September 2, 1997, the disclosure of which is hereby incorporated in its entirety by this reference. Mask layer 18 is formed on stacked capacitor structure 10 by dispensing a mask material onto stacked capacitor structure 10 while spinning the substrate bearing stacked capacitor structure 10 relative to an axis perpendicular to a plane of the substrate bearing stacked capacitor structure 10 at a first speed, which is preferably an optimum speed for forming a substantially homogeneous film from the mask material. When a substantially homogeneous film of mask material has been formed on stacked capacitor structure 10, the rate at which stacked capacitor structure 10 is spun is decreased to a second speed. The second speed and the duration at which stacked capacitor structure 10 is spun at the second speed permits the mask material to flow into and to begin to set within containers 14 of stacked capacitor structure 10. The rate of spinning stacked capacitor structure 10 is then gradually increased, or ramped up, to a third speed, which is maintained until a film of mask material covering surface 12 reaches a desired, reduced thickness. The rate at which stacked capacitor structure 10 is spun may again be reduced to further permit the mask material to set. A bead of the mask material formed around the periphery of a substrate (e.g., a wafer) including stacked capacitor structure 10 may be

removed by known processes to provide a substantially planar surface over stacked capacitor structure. The substrate including stacked capacitor structure 10 may also be spun again to begin removing solvents from the mask material. Mask layer 18 is then subjected to a soft bake, as known in the art, to substantially remove solvents from the mask material.

By way of example, when ARCH 895 photoresist is used as the mask material, the substrate bearing stacked capacitor structure 10 is spun at a first speed of about 1,000 rpm until a substantially homogeneous layer is formed (e.g., about one second to about five seconds). The spinning rate is then decreased to about 100 rpm for a period of about five seconds to about ten seconds to allow the photoresist within containers 14 to begin setting. The rate at which stacked capacitor structure 10 is spun is then gradually increased to a third speed of at least about 1,500 rpm until the photoresist covering surface 12 reaches a desired, reduced thickness or until photoresist is substantially removed from surface 12. The spin rate is then decreased again, this time to about 50 rpm, for a duration of about 19 to about 50 seconds to permit additional setting, or casting, of the photoresist. Such additional spinning creates a bead of photoresist near an edge of a substrate of which stacked capacitor structure 10 is a part. Known edge bead removal techniques are employed to remove this bead from the edge of the substrate and to provide a substantially planar surface. Any solvent remaining in the photoresist is then substantially removed therefrom by gradually increasing the rate at which stacked capacitor structure 10 is spun to about 5,000 rpm. Mask layer 18 is then subjected to a known soft bake process, preferably at a temperature of about 100° C. to about 150° C. to substantially remove solvents from the photoresist.

Referring now to FIG. 3, once a mask layer 18 with a substantially planar surface 19 of is formed, the portions of mask layer 18 and of hemispherical grain silicon layer 16 that are located above a plane of surface 12 are removed from stacked capacitor structure 10. In order to reduce or eliminate the creation of potentially contaminating debris and of surface defects that may be caused by mechanical planarization processes, layers 18 and 16 are removed by known chemical processes, such as dry etch processes or wet etch, or wet dip, processes. For example, mask layer 18 may be selectively removed

by use of a known resist strip, then layer 16 removed from surface 12 with a wet etchant that removes silicon with selectivity over the portions of mask layer 18 remaining in containers 14 and over an underlying dielectric layer 15. As another example, layers 18 and 16 may be substantially concurrently removed with an etchant or combination of etchants that will remove mask layer 18 and hemispherical grain silicon layer 16 at substantially the same rates. Mask material remaining in containers 14 may then be removed by known processes, such as the use of known wet or dry strip materials (e.g., an ammonium hydroxide (NH_4OH) dry strip known in the art as a "piranha" strip when the mask material is ARCH 895 or a similar photoresist). This process provides a stacked capacitor structure 10 with conductively doped hemispherical grain silicon 16-lined containers 14 recessed in a substantially defect and contaminant free surface 12 of dielectric layer 15, as shown in FIG. 4. Stacked capacitor structure 10 shown in FIG. 4 may then be processed as known in the art to fabricate a finished stacked capacitor.

Turning now to FIGs. 5 and 6, another embodiment of a semiconductor device structure, in this instance a shallow trench isolation structure 20, incorporating teachings of the present invention is illustrated. FIG. 5 depicts a shallow trench isolation structure 20 that includes a semiconductor substrate 21 formed from silicon, gallium arsenide, indium phosphide, or another suitable semiconductor material, and which may be in the form of a wafer or another substrate, such as a silicon-on-glass, silicon-on-sapphire, silicon-on-ceramic, or other silicon-on-insulator type substrate. Semiconductor substrate 21 includes a surface 22 with one or more trenches 24 recessed, or formed, therein. Trenches 24 may be formed in semiconductor substrate 21 by known techniques, such mask and etch processes. Shallow trench isolation structure 20 also includes a mask layer 28 with a substantially planar surface 29. Mask layer 28 substantially fills trenches 24 and may also cover surface 22 of semiconductor substrate. As shown in FIG. 5, the thickness T′ of portions of mask layer 28 overlying surface 22 is less than the depth D′ of trenches 24. Preferably, thickness T′ is less than about half of depth D′. Alternatively, surface 22 may remain substantially uncovered by mask layer 28. Mask layer 28 may be formed from a photoresist or other polymer by the same or similar

processes to those described previously herein with reference to the fabrication of mask layer 18 illustrated in FIG. 2.

FIG. 6 illustrates the implantation of a conductivity dopant C, such as a known p-type or n-type conductivity dopant (e.g., phosphorus (P), boron (B), arsenic (As), or antimony (Sb)), into shallow trench isolation structure 20 through mask layer 28. Conductivity dopant C is prevented from passing through the thicker regions of mask layer 28 into regions 25 of semiconductor substrate 21 located at the bottoms of trenches 24. Conductivity dopant C does, however, pass through thinner areas of mask layer 28 that are located on surface 22 or to exposed areas of surface 22 so as to conductively dope regions 23 of semiconductor substrate 21 continuous with surface 22, which regions lie laterally adjacent trenches 24. Once regions 23 have been conductive doped, mask layer 28 may be removed from trenches 24 and surface 22 (if necessary) to facilitate completion of shallow trench isolation structure 20, as well as the fabrication of semiconductor devices thereon.

Referring now to FIGs. 7-11, a second shallow trench isolation structure 30 embodiment of a semiconductor device structure according to the present invention is illustrated. With reference to FIGs. 7 and 8, shallow trench isolation structure 30 includes a semiconductor substrate 21 with a surface 22 and trenches 24 recessed, or formed in, surface 22. A layer of electrically nonconductive material, or insulator layer 36, substantially fills trenches 24 and covers surface 22. Insulator layer 36 has a nonplanar upper surface 37 and includes valleys 34 located substantially above trenches 24 and peaks 32 located substantially above surface 22.

Shallow trench isolation structure 30 may also have a layer 38, 38′ of stress buffer material, which is also referred to herein as a stress buffer layer, having a substantially planar surface 39 disposed at least partially over insulator layer 36. FIG. 7 illustrates stress buffer layer 38, which substantially fills valleys 34 recessed in insulator layer 36 and substantially completely covers peaks 32. The thickness T″ of regions of stress buffer layer 38 located above peaks 32 is less than the depths D″ of valleys 34. Thickness T″ is preferably less than about half of depth D″. FIG. 8 depicts stress buffer layer 38′, which does not extend over peaks 32 and which may only partially fill valleys

34. Stress buffer layers 38, 38′ are preferably formed from a photoresist or other polymer by the same or similar processes to those disclosed previously herein with reference to the fabrication of mask layer 18 illustrated in FIG. 2.

Once a substantially planar surface is formed over shallow trench isolation structure 30, such as that formed at least partially by surface 39 of stress buffer layer 38 and as illustrated in FIG. 7, stress buffer layer 38 and portions of insulator layer 36 located above the plane of surface 22 may be substantially concurrently removed. For example, layers 38 and 36 may be substantially removed by exposure to the same etchant or combination of etchants that will remove stress buffer layer 38 and insulator layer 36 at substantially the same rates to provide the finished shallow trench isolation structure 30 illustrated in FIG. 11. Either wet etchants or dry etchants may be used. Preferably, the use of etchants eliminates the formation of imperfections or defects in surface 22 of semiconductor substrate 21, as well as the possible introduction of contaminants or other debris thereon. Alternatively, known chemical-mechanical planarization processes may be used to substantially concurrently remove stress buffer layer 38 and portions of insulator layer 36 above surface 22, also providing a finished shallow trench isolation structure 30 such as that illustrated in FIG. 11. As stress buffer layer 38 provides a substantially planar surface over shallow trench isolation structure 30, the likelihood that material of insulator layer 36 will be broken off during the chemical-mechanical planarization process is reduced, thereby reducing the formation of imperfections or defects in surface 22, as well as the creation of contaminants or other debris, which may occur during chemical-mechanical planarization of a nonplanar surface.

As shown in FIG. 8, stress buffer layer 38′ may not provide shallow trench isolation structure 30 with a substantially planar surface. Rather, peaks 32 of insulator layer 36 protrude above surface 39′ of stress buffer layer 38′. In order to provide a substantially planar surface over shallow trench isolation structure 30, the portions of peaks 32 that protrude above the plane of surface 39′ may be selectively removed, such as by use of selective wet or dry etch processes. The material of peaks 32 that protrudes above the plane of surface 39′ is removed at least until a substantially planar surface 31 is formed over shallow trench isolation structure 30, as depicted in FIG. 9.

As illustrated in FIG. 10, the selective removal of material forming insulator layer 36 may continue until portions of insulator layer 36 located above the plane of surface 22 are substantially removed. As a result, discontinuous quantities of stress buffer layer 38′ remain above trenches 24 and the portions of insulator layer 36 remaining therein. Stress buffer layer 38′ may be removed mechanically or by use of a wet or dry etchant that will not substantially remove or react with the materials of semiconductor substrate 21 or of the portions of insulator layer 36 remaining within trenches 24. For example, if a photoresist is used to form stress buffer layer 38′, known resist strippers may be used to remove stress buffer layer 38′ to form a finished shallow trench isolation structure 30, such as that illustrated in FIG. 11.

Alternatively, once a substantially planar surface 31 has been formed over shallow trench isolation structure 30, as shown in FIG. 9, stress buffer layer 38′ and the portions of insulator layer 36 located above the plane of surface 22 may be substantially concurrently removed from above shallow trench isolation structure by use of one or more dry or wet etchants that remove the materials of layers 38 and 36 at substantially the same rates, as known in the art, or by known chemical mechanical planarization processes to provide the finished shallow trench isolation structure 30 illustrated in FIG. 11.

Once a finished shallow trench isolation structure 30, such as that depicted in FIG. 11, has been fabricated, one or more semiconductor devices may then be fabricated on shallow trench isolation structure 30, as known in the art.

FIGs. 12-16 illustrate yet another embodiment of a semiconductor device structure 40 that incorporates teachings of the present invention. With reference to FIGs. 12 and 13, semiconductor device structure 40 includes dual damascene trenches 44 formed in a surface 42 of an insulator layer 41 thereof. A conductive layer 46 overlies surface 42 and substantially fills trenches 44. Conductive layer 46 has a nonplanar upper surface 47 that includes valleys 54 located substantially over trenches 44 and peaks 52 located substantially over surface 42. Insulator layer 41, trenches 44, and conductive layer 46, as well as other structures of semiconductor device structure 40 underlying insulator layer 41 and trenches 44 are each fabricated by known processes, such as those

disclosed in U.S. Patent 5,980,657 to Farrar et al. on November 9, 1999, the disclosure of which is hereby incorporated in its entirety by this reference.

Semiconductor device structure 40 also includes a layer of stress buffer material, which is also referred to herein as a stress buffer layer 48, 48′, at least partially covering conductive layer 46 and having a substantially planar surface 49, 49′. FIG. 12 illustrates stress buffer layer 48, which substantially fills valleys 54 recessed in conductive layer 46 and substantially completely covers peaks 52. The thickness T‴ of regions of stress buffer layer 48 located above peaks 52 is less than the depths D‴ of valleys 54. Thickness T‴ is preferably less than about half of depth D‴. FIG. 13 depicts stress buffer layer 48′, which does not extend over peaks 52 and which may only partially fill valleys 54. Stress buffer layers 48, 48′ are preferably formed from a photoresist or other polymer by the same or similar processes to those disclosed previously herein with reference to the fabrication of mask layer 18 illustrated in FIG. 2.

Once a substantially planar surface is formed over semiconductor device structure 40, such as that formed at least partially by surface 49 of stress buffer layer 48 and as illustrated in FIG. 12, stress buffer layer 48 and portions of conductive layer 46 located above the plane of surface 42 may be substantially concurrently removed. For example, layers 48 and 46 may be substantially concurrently removed with an etchant or combination of etchants that will remove stress buffer layer 48 and insulator layer 46 at substantially the same rates to provide the finished semiconductor device structure 40 illustrated in FIG. 16. Either wet etchants or dry etchants may be used. Preferably, the use of etchants eliminates the formation of imperfections or defects in surface 42 of insulator layer 41, as well as the possible introduction of contaminants or other debris thereon. Alternatively, known chemical-mechanical planarization processes may be used to substantially concurrently remove stress buffer layer 48 and portions of conductive layer 46 above surface 42, also providing a finished semiconductor device structure 40 such as that illustrated in FIG. 16. As stress buffer layer 48 provides a substantially planar surface over shallow trench isolation structure 40, the likelihood that material of conductive layer 46 will be broken off during the chemical-mechanical planarization process is reduced, thereby reducing the formation of imperfections or defects in surface

42, as well as the creation of contaminants or other debris, which may occur during chemical-mechanical planarization of a nonplanar surface.

As illustrated in FIG. 13, stress buffer layer 48′ may not provide semiconductor device structure 40 with a substantially planar surface. Rather, peaks 52 of conductive layer 46 protrude above surface 49′ of stress buffer layer 48′. In order to provide a substantially planar surface over semiconductor device structure 40, the portions of peaks 52 that protrude above the plane of surface 49′ may be selectively removed, such as by use of selective wet or dry etch processes. The material of peaks 52 that protrudes above the plane of surface 49′ is removed at least until a substantially planar surface 51 is formed over semiconductor device structure 40, as depicted in FIG. 14.

FIG. 15 illustrates that the selective removal of material forming conductive layer 46 may continue until portions of conductive layer 46 located above the plane of surface 42 are substantially removed therefrom. As a result, discontinuous quantities of stress buffer layer 48′ remain above trenches 44 and the portions of conductive layer 46 remaining therein. Stress buffer layer 48′ may be removed mechanically or by use of a wet or dry etchant that will not substantially remove or react with the materials of insulator layer 41 or of the portions of conductive layer 46 remaining within trenches 44. For example, if a photoresist is used to form stress buffer layer 48′, known resist strippers may be used to remove stress buffer layer 48′ to form a semiconductor device structure 40 such as that illustrated in FIG. 16.

Alternatively, once a substantially planar surface 51 has been formed over semiconductor device structure 40, as shown in FIG. 14, stress buffer layer 48′ and the portions of conductive layer 46 located above the plane of surface 42 may be substantially concurrently removed from above shallow trench isolation structure by use of one or more wet or dry etchants that remove the materials of layers 48 and 46 at substantially the same rates, as known in the art, or by known chemical mechanical planarization processes to provide the semiconductor device structure 40 illustrated in FIG. 16.

Once a semiconductor device structure 40 such as that depicted in FIG. 16 has been fabricated, further known fabrication processes may be performed.

Although the foregoing description contains many specifics, these should not be construed as limiting the scope of the present invention, but merely as providing illustrations of some of the presently preferred embodiments. Similarly, other embodiments of the invention may be devised which do not depart from the spirit or scope of the present invention. Features from different embodiments may be employed in combination. The scope of the invention is, therefore, indicated and limited only by the appended claims and their legal equivalents, rather than by the foregoing description. All additions, deletions and modifications to the invention as disclosed herein which fall within the meaning and scope of the claims are to be embraced thereby.

CLAIMS

What is claimed is:

1. A method for disposing a material on a semiconductor device structure, comprising:

providing a semiconductor device structure including a surface and at least one recess formed in said surface;

disposing the material on said surface so as to substantially fill said at least one recess, the material covering said surface having a thickness less than a depth of said at least one recess without subsequently removing the material from over said surface.

2. The method of claim 1, wherein said disposing comprises disposing the material so as to substantially fill the at least one recess without substantially covering said surface.

3. The method of claim 1, wherein said disposing comprises:

applying the material to said surface of said semiconductor device structure;

spinning said semiconductor device structure;

decreasing a rate of said spinning while permitting the material to at least partially cure; and

gradually increasing said rate of said spinning.

4. The method of claim 3, further comprising exposing the material to a soft baking temperature following said gradually increasing.

5. The method of claim 3, wherein said spinning is effected at a rate of about 1,000 rpm.

6. The method of claim 3, wherein said decreasing said rate comprises decreasing said rate of said spinning to about 100 rpm.

7. The method of claim 3, wherein said gradually increasing said rate comprises gradually increasing said rate of said spinning to at least about 1,000 rpm.

8. The method of claim 1, wherein, upon exposing the material disposed over an entirety of said semiconductor device structure to an etchant, the material covering said surface is substantially removed therefrom, while the material located in said at least one recess substantially fills said at least one recess.

9. The method of claim 1, wherein said providing said semiconductor device structure comprises providing a stacked capacitor structure with said at least one recess comprising at least one container formed in an insulator layer of said stacked capacitor structure, said surface and said at least one container being lined with a conductive material.

10. The method of claim 9, wherein said providing said semiconductor device structure comprises providing said stacked capacitor structure with said surface and said at least one container being lined with doped hemispherical grain polysilicon.

11. The method of claim 9, wherein said disposing the material comprises disposing a mask material over said semiconductor device structure.

12. The method of claim 1, wherein said providing said semiconductor device structure comprises providing a shallow trench isolation structure with said at least one recess comprising at least one trench formed in a surface of said shallow trench isolation structure.

13. The method of claim 12, wherein said disposing the material comprises disposing a mask material over the shallow trench isolation structure.

14. The method of claim 12, wherein said providing comprises providing said shallow trench isolation structure with an insulator layer substantially filling said at least one trench and covering said surface.

15. The method of claim 14, wherein said disposing the material comprises disposing a stress buffer over said insulator layer, said stress buffer having a substantially planar surface without removing material thereof following said disposing.

16. The method of claim 1, wherein said providing comprises providing a semiconductor device structure having a surface with at least one dual damascene trench recessed therein and a layer of conductive material with a nonplanar surface disposed in said at least one dual damascene trench and at least partially covering said surface.

17. The method of claim 16, wherein said disposing the material comprises disposing a stress buffer over said layer of conductive material, said stress buffer having a substantially planar surface without removing material thereof following said disposing.

18. A method for masking a stacked capacitor structure, comprising:

providing a semiconductor device structure with a stacked capacitor structure including:

an insulator layer;

at least one container formed in said insulator layer; and

a layer of conductive material covering a surface of said insulator layer and lining said at least one container;

applying a layer of masked material to said semiconductor device structure; and

spreading said mask material across said semiconductor device structure so as to substantially fill said at least one container and cover said layer of conductive material over said surface with a thickness of about less than half a depth of said at least one container.

19. The method of claim 18, wherein said providing said semiconductor device structure comprises providing a semiconductor device structure with said layer of conductive material of said stacked capacitor structure comprising hemispherical grain polysilicon.

20. The method of claim 18, wherein said spreading comprises spinning said mask material across said semiconductor device structure.

21. The method of claim 20, wherein said spinning comprises:
rotating said semiconductor device structure at a first speed;
decreasing a rate of said rotating to a second speed; and
gradually increasing said rate of said rotating to a third speed.

22. The method of claim 21, wherein said decreasing said rate follows said rotating.

23. The method of claim 22, wherein said gradually increasing said rate follows said decreasing said rate.

24. The method of claim 18, wherein said spreading comprises substantially filling said at least one container with said mask material while leaving said layer of conductive material over said surface substantially uncovered by said mask material.

25. The method of claim 18, further comprising removing said layer of conductive material located over said surface.

26. The method of claim 25, wherein said removing comprises etching said layer of conductive material.

27. The method of claim 26, wherein said etching comprises wet etching said layer of conductive material.

28. The method of claim 26, wherein said etching comprises dry etching said layer of conductive material.

29. The method of claim 25, wherein during said removing said at least one container remains substantially filled with said mask material.

30. The method of claim 25, further comprising removing said mask material from said at least one container.

31. A method for forming a shallow trench isolation structure, comprising:

providing a semiconductor substrate with a surface and at least one shallow trench recessed in said surface;

applying mask material to said semiconductor substrate;

spreading said mask material across said semiconductor substrate so as to substantially fill said at least one trench, said mask material covering said surface as a result of said spreading having a thickness of less than about half a depth of said at least one shallow trench; and

exposing at least said mask to a dopant so as to conductively dope semiconductor material beneath said surface without substantially doping semiconductor material located beneath said at least one trench.

32. The method of claim 31, wherein said spreading comprises spinning said mask material across said semiconductor substrate.

33. The method of claim 32, wherein said spinning comprises:
rotating said semiconductor substrate at a first speed;
decreasing a rate of said rotating to a second speed; and
gradually increasing said rate of said rotating to a third speed.

34. The method of claim 33, wherein said decreasing said rate follows said rotating.

35. The method of claim 34, wherein said gradually increasing said rate follows said decreasing said rate.

36. The method of claim 31, wherein said spreading comprises substantially filling said at least one trench with said mask material while leaving said surface substantially uncovered by said mask material.

37. The method of claim 31, wherein said exposing includes implanting conductivity dopant into regions of said semiconductor substrate continuous with said surface without implanting conductivity dopant into regions of said semiconductor substrate continuous with a bottom of said at least one trench.

38. The method of claim 31, further comprising removing said mask material from said semiconductor substrate.

39. A method for fabricating a semiconductor device structure, comprising:
providing a semiconductor device structure with a surface, at least one recess formed in said surface, and a material at least partially coving said surface and substantially filling said at least one recess, said material layer having a nonplanar surface;
applying a stress buffer material to said material layer; and
spreading said stress buffer material over said material layer so as to impart said stress buffer material with a substantially planar surface without subsequently planarizing said stress buffer material.

40. The method of claim 39, wherein said providing comprises providing said semiconductor device structure with said nonplanar surface of said material layer including at least one peak located substantially over said surface and at least one valley located substantially over said at least one recess.

41. The method of claim 39, wherein said spreading comprises spinning said stress buffer material across said semiconductor device structure.

42. The method of claim 41, wherein said spinning comprises:
rotating said semiconductor device structure at a first speed;
decreasing a rate of said rotating to a second speed; and
gradually increasing said rate of said rotating to a third speed.

43. The method of claim 42, wherein said decreasing said rate follows said rotating.

44. The method of claim 43, wherein said gradually increasing said rate follows said decreasing said rate.

45. The method of claim 40, wherein said spreading comprises at least partially filling said at least one valley with said stress buffer material while leaving said at least one peak substantially uncovered by said stress buffer material.

46. The method of claim 45, further comprising planarizing at least said material layer.

47. The method of claim 46, wherein said planarizing comprises etching at least one region of said material layer exposed through said stress buffer material with selectivity over said stress buffer material.

48. The method of claim 47, wherein said etching is effected until a surface of said at least one region is in substantially the same plane as said surface of said stress buffer material.

49. The method of claim 48, wherein said planarizing further comprises abrasive planarizing said stress buffer material and said at least one region to expose said surface adjacent said at least one recess, said surface and a surface of material in said at least one recess being located in substantially the same plane following said planarizing.

50. The method of claim 48, wherein said planarizing further comprises concurrently etching said material layer and said stress buffer material at substantially the same rate so as to expose said surface adjacent said at least one recess with said surface and a surface of material in said at least one recess being located in substantially the same plane following said planarizing.

51. The method of claim 47, wherein said etching is effected until said surface of said semiconductor device structure is exposed through said material layer.

52. The method of claim 51, wherein said etching is effected until a surface of material in said at least one recess is in substantially the same plane as said surface.

53. The method of claim 51, further comprising removing said stress buffer material from said semiconductor device structure.

54. The method of claim 40, wherein said spreading comprises forming a substantially planar surface over said semiconductor device structure.

55. The method of claim 54, further comprising planarizing at least said material layer.

56. The method of claim 55, wherein said planarizing comprises substantially concurrently abrasive planarizing said stress buffer material and said material layer to expose said surface adjacent said at least one recess, said surface and a surface of material in said at least one recess being located in substantially the same plane following said planarizing.

57. The method of claim 55, wherein said planarizing comprises substantially concurrently etching said material layer and said stress buffer material at substantially the same rate so as to expose said surface adjacent said at least one recess with said surface and a surface of material in said at least one recess being located in substantially the same plane following said planarizing.

58. The method of claim 39, wherein said providing said semiconductor device structure comprises providing a shallow trench isolation structure with said at least one recess comprising at least one trench and said material layer comprising electrical insulator material.

59. The method of claim 39, wherein said providing comprises providing a semiconductor device structure with said at least one trench comprising a dual damascene trench and said material layer comprising conductive material.

60. A method for preparing a surface of a semiconductor device structure for planarization, comprising:

providing a semiconductor device structure including at least one recess formed in a surface thereof and a first material layer substantially filling said at least one recess and covering said surface, said first material layer having a nonplanar surface;

applying a second material to said first material layer; and

spreading said second material over said first material layer so as to form a second material layer having a substantially planar surface without requiring subsequent planarization of said second material.

61. The method of claim 60, wherein said applying said second material comprises applying a layer of stress buffer material to said first material layer.

62. The method of claim 60, wherein said spreading comprises:

spinning said semiconductor device structure at a first speed;

gradually decreasing a rate of said spinning to a second speed; and

gradually increasing a rate of said spinning to a third speed.

63. The method of claim 62, wherein spinning said semiconductor device structure at said second speed comprises permitting said second material within said at least one recess to at least partially set.

64. The method of claim 62, wherein spinning said semiconductor device structure at said third speed comprises forming said second material over said surface to a desired thickness.

65. The method of claim 60, wherein said providing comprises providing a shallow trench isolation structure with said at least one recess comprising at least one trench formed in a surface of said shallow trench isolation structure.

66. The method of claim 65, wherein said providing further comprises providing a shallow trench isolation structure with said first material layer comprising an electrical insulator material.

67. The method of claim 60, wherein said providing comprises providing a semiconductor device structure with said at least one recess comprising at least one dual damascene trench formed therein.

68. The method of claim 67, wherein said providing further comprises providing a semiconductor device structure with said first material layer comprising conductive material.

69. The method of claim 61, wherein said spreading comprises at least partially filling at least one valley of said first material layer with said stress buffer material while leaving at least one peak of said first material layer substantially uncovered by said stress buffer material.

70. The method of claim 69, further comprising planarizing at least said first material layer.

71. The method of claim 70, wherein said planarizing comprises etching at least one region of said first material layer exposed through said stress buffer material with selectivity over said stress buffer material.

72. The method of claim 71, wherein said etching is effected until a surface of said at least one region is in substantially the same plane as said surface of said stress buffer material.

73. The method of claim 72, wherein said planarizing further comprises abrasive planarizing said stress buffer material and said at least one region to expose said surface adjacent said at least one recess, said surface and a surface of first material in said at least one recess being located in substantially the same plane following said planarizing.

74. The method of claim 72, wherein said planarizing further comprises concurrently etching said first material layer and said stress buffer material at substantially the same rate so as to expose said surface adjacent said at least one recess with said surface and a surface of first material in said at least one recess being located in substantially the same plane following said planarizing.

75. The method of claim 71, wherein said etching is effected until said surface of said semiconductor device structure is exposed through said first material layer.

76. The method of claim 75, wherein said etching is effected until a surface of first material in said at least one recess is in substantially the same plane as said surface.

77. The method of claim 75, further comprising removing said stress buffer material from said semiconductor device structure.

78. The method of claim 61, wherein said spreading comprises forming a substantially planar surface over said semiconductor device structure.

79. The method of claim 78, further comprising planarizing at least said first material layer.

80. The method of claim 79, wherein said planarizing comprises substantially concurrently abrasive planarizing said stress buffer material and said first material layer to expose said surface adjacent said at least one recess, said surface and a surface of first material in said at least one recess being located in substantially the same plane following said planarizing.

81. The method of claim 79, wherein said planarizing comprises substantially concurrently etching said first material layer and said stress buffer material at substantially the same rate so as to expose said surface adjacent said at least one recess with said surface and a surface of first material in said at least one recess being located in substantially the same plane following said planarizing.

82. A spin coating method, comprising:
applying a material to a substrate;
spinning said substrate and said material at a first speed;
decreasing a rate of said spinning to a second speed; and
gradually increasing a rate of said spinning to a third speed.

83. The method of claim 82, wherein said spinning said substrate and said material at said first speed comprises substantially filling recesses formed in said substrate with said material.

84. The method of claim 82, wherein said gradually decreasing said rate and spinning said substrate and said material at said second speed comprise permitting said material located within recesses formed in said substrate to set.

85. The method of claim 82, wherein spinning said substrate and said material at said third speed comprises forming said material over a surface of said substrate to a desired thickness.

86. The method of claim 82, wherein said gradually decreasing said rate follows said spinning.

87. The method of claim 84, wherein said gradually increasing said rate follows said decreasing said rate.

88. A semiconductor device structure with a substantially planar surface, comprising:

a substrate including at least one recess formed therein; and

a material layer disposed over said substrate and substantially filling said at least one recess, said material layer having substantially planar surface free of abrasive planarization-induced defects.

89. The semiconductor device structure of claim 88, wherein said substrate comprises a semiconductor substrate with a surface and said at least one recess comprising at least one trench recessed in said surface.

90. The semiconductor device structure of claim 88, wherein said material layer comprises a mask material.

91. The semiconductor device structure of claim 90, further comprising at least one conductively doped region continuous with said surface and laterally adjacent said at least one trench.

92. The semiconductor device structure of claim 88, wherein said substrate comprises:

a shallow trench isolation structure including a semiconductor substrate with a surface and at least one trench formed in said surface; and

an insulator layer substantially filling said at least one trench and covering said surface.

93. The semiconductor device structure of claim 92, wherein said insulator layer includes a nonplanar upper surface with at least one peak located substantially above said surface and at least one valley located substantially above said at least one trench.

94. The semiconductor device structure of claim 93, wherein said material layer comprises a stress buffer layer that substantially fills said at least one valley in said insulator layer.

95. The semiconductor device structure of claim 88, wherein said substrate comprises:

a semiconductor device structure including a surface with at least one dual damascene trench formed in said surface; and

a conductive layer substantially filling said at least one dual damascene trench and covering said surface.

96. The semiconductor device structure of claim 95, wherein said conductive layer includes a nonplanar upper surface with at least one peak located substantially above said surface and at least one valley located substantially above said at least one trench.

97. The semiconductor device structure of claim 96, wherein said material layer comprises a stress buffer layer that substantially fills said at least one valley in said insulator layer.

98. The semiconductor device structure of claim 88, wherein said substrate comprises a stacked capacitor structure including an insulator layer with at least one container recessed therein.

99. The semiconductor device structure of claim 98, wherein said material layer comprises a mask material, said mask material substantially filling said at least one container.

100. The semiconductor device structure of claim 99, wherein said mask material covering a surface of said insulator layer has a thickness less than a height of said at least one container.

101. The semiconductor device structure of claim 99, wherein said mask material covering a surface of said insulator layer has a thickness of less than about half a depth of said at least one container.

ABSTRACT

A method spinning a material onto a semiconductor device structure so as to substantially fill recesses formed in a surface of the semiconductor device structure and to impart the material with a substantially planar surface and semiconductor device structures formed thereby. The thickness of the material covering the surface is less than the depth of the recesses. The surface may remain substantially uncovered by the material.

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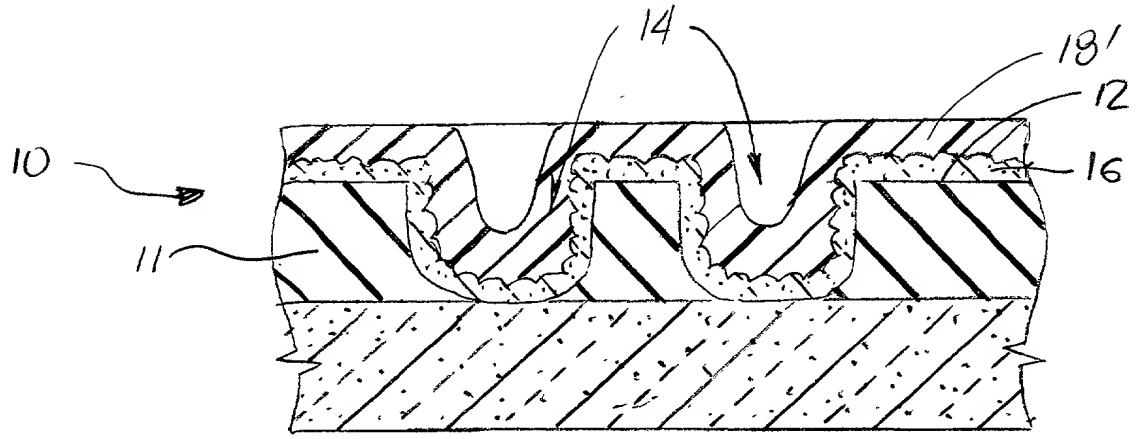

FIG. 1

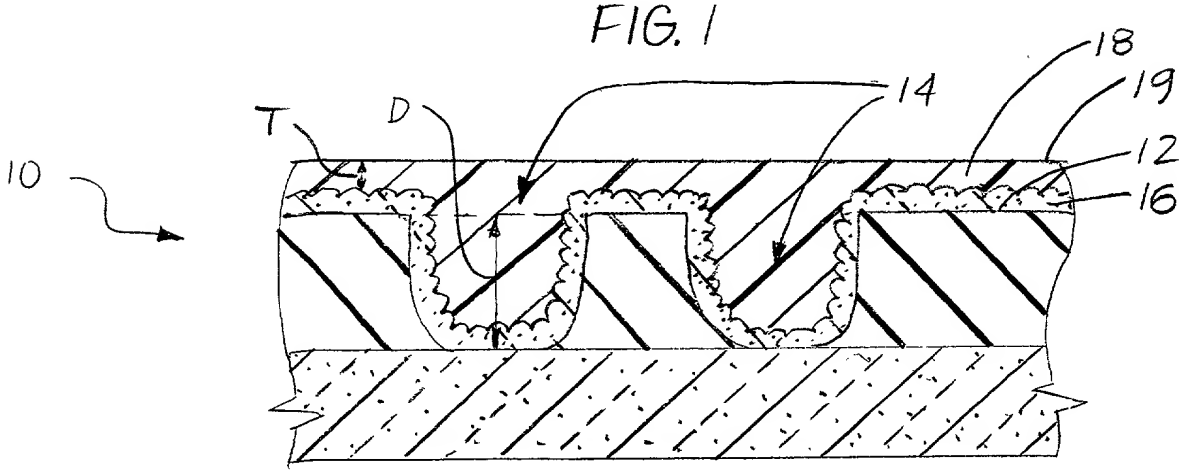

FIG. 2

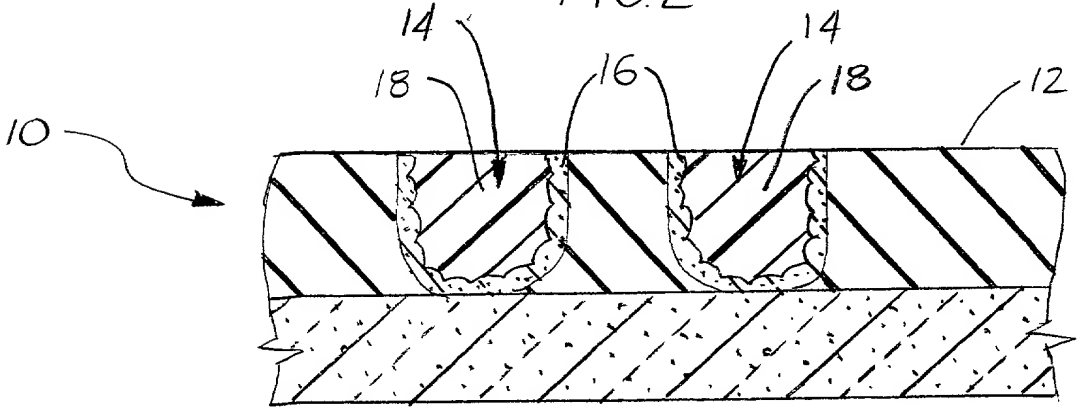

FIG. 3

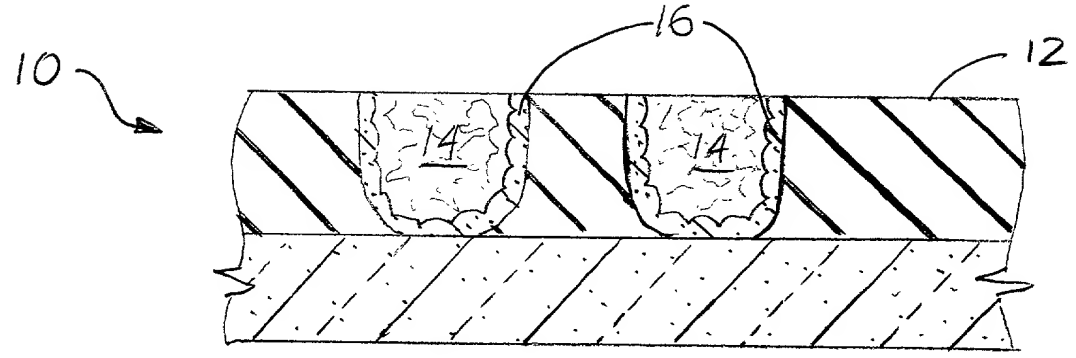

FIG. 4

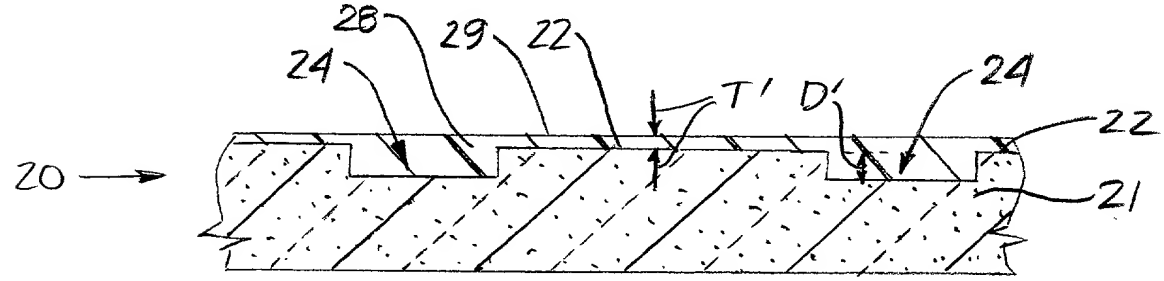

FIG. 5

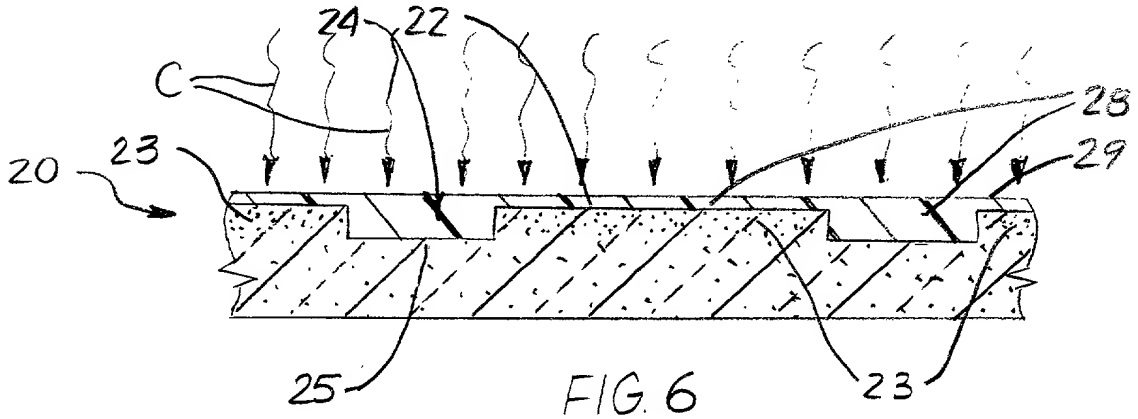

FIG. 6

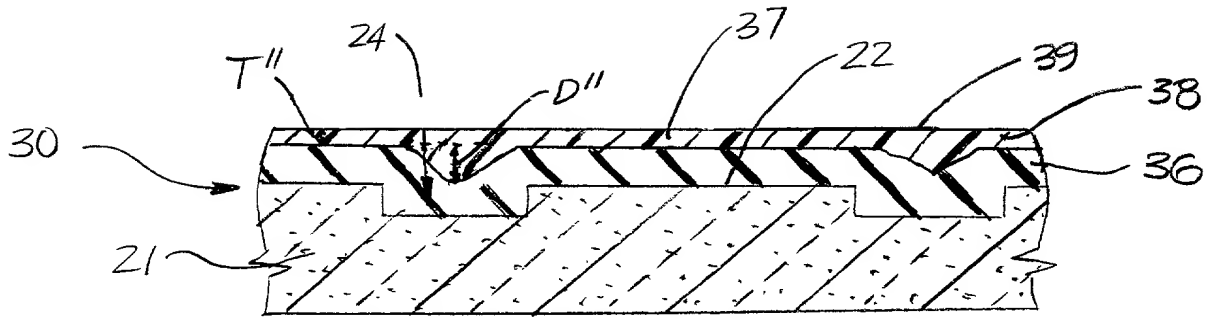

FIG. 7

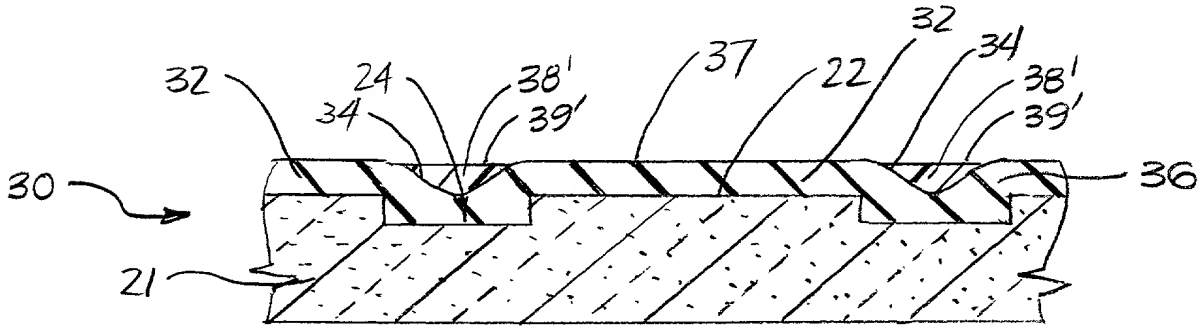

FIG. 8

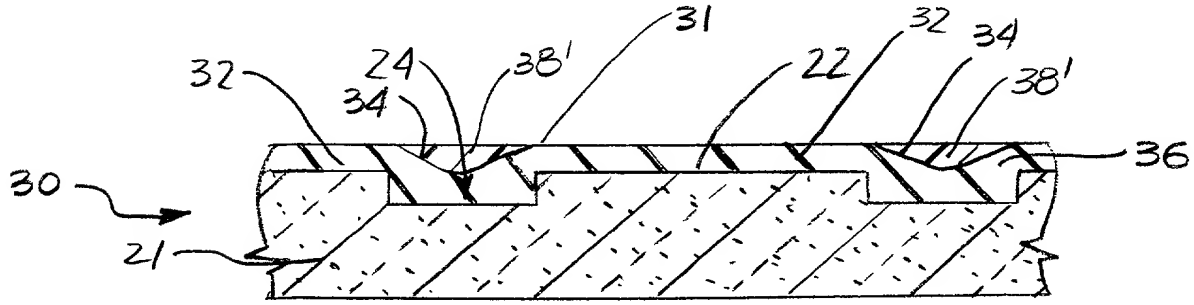

FIG. 9

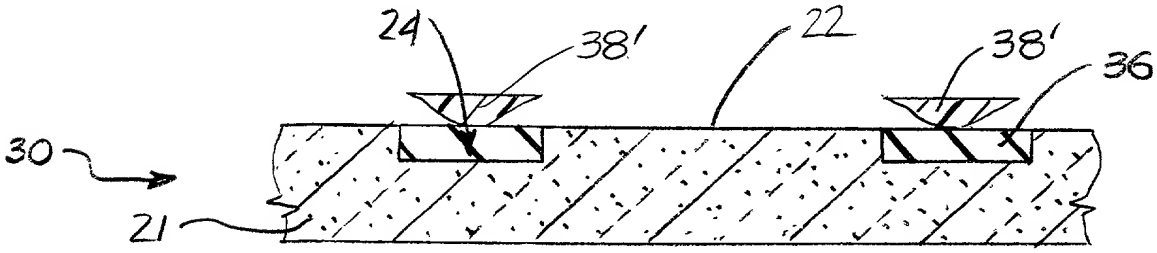

FIG. 10

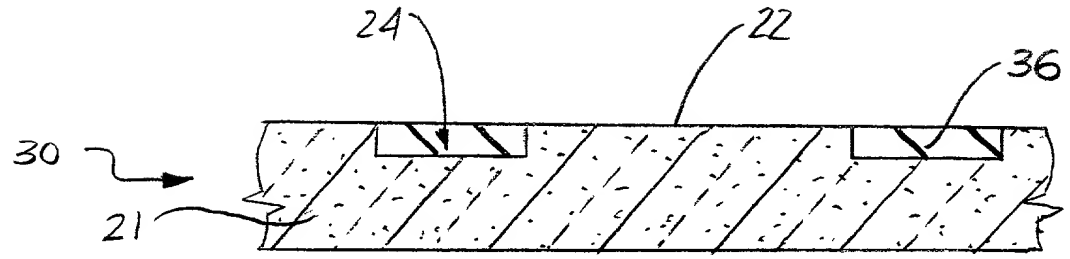

FIG. 11

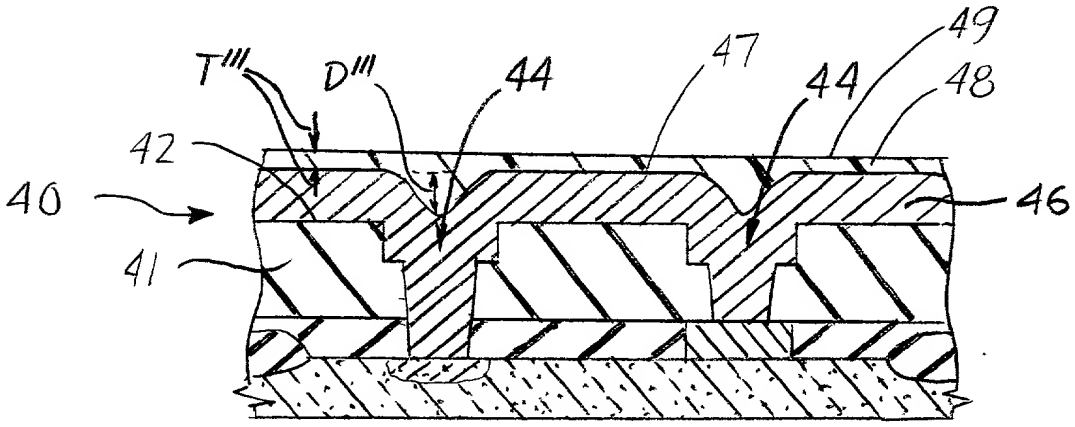

FIG. 12

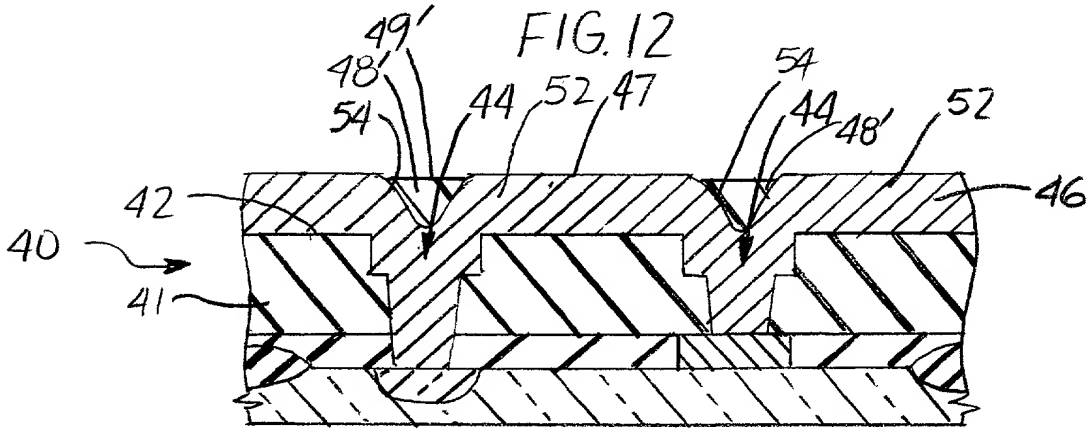

FIG. 13

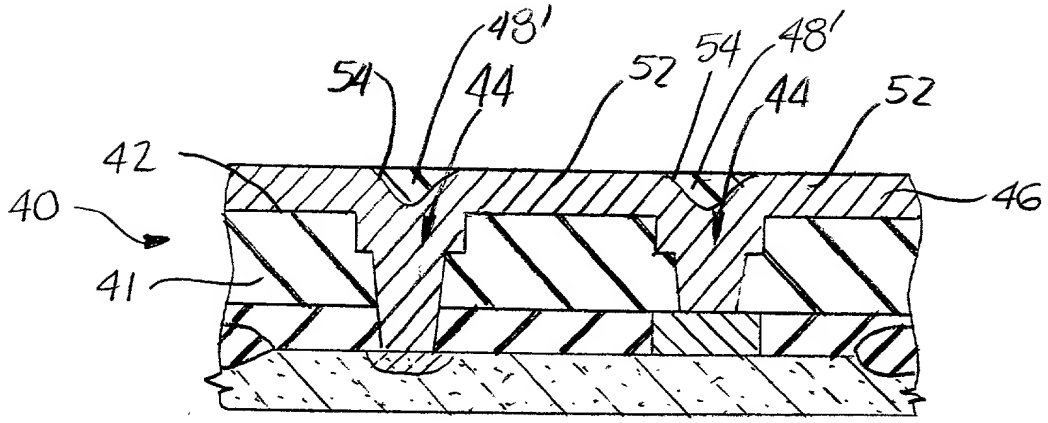

FIG. 14

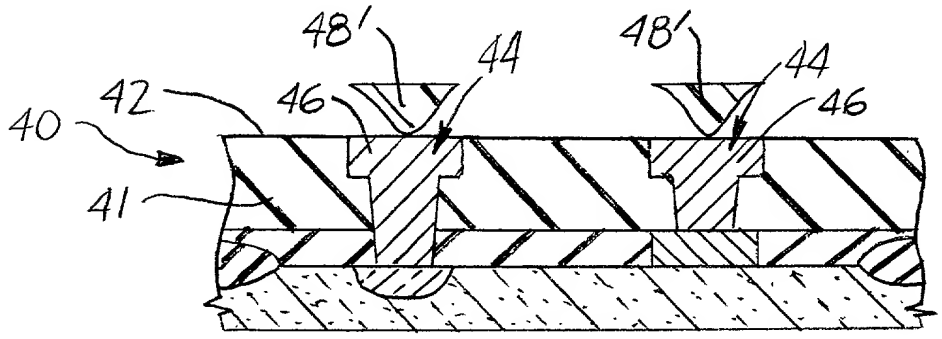

FIG. 15

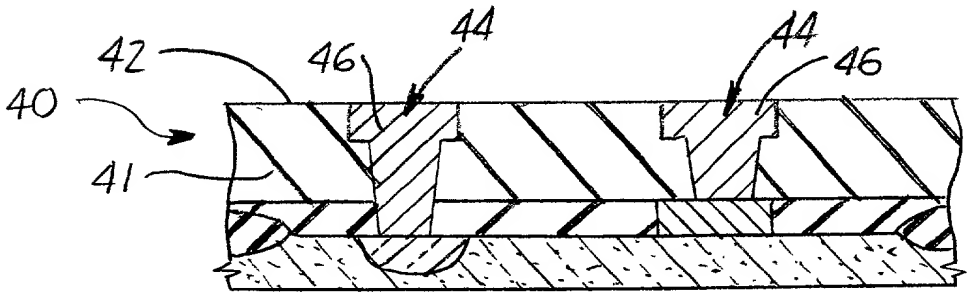

FIG. 16

DECLARATION FOR PATENT APPLICATION (WITH POWER OF ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled SPIN COATING FOR MAXIMUM FILL CHARACTERISTIC YIELDING A PLANARIZED THIN FILM SURFACE, the specification of which (check one):

- ☒ is attached hereto.
- ☐ was filed on _____ as United States application serial no. _____ and was amended on _____.
- ☐ was filed on _____ as PCT international application no. _____ and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

			Priority Claimed	
(number)	(country)	(day/month/year filed)	Yes	No
(number)	(country)	(day/month/year filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application.

(application serial no.)	(filing date)	(status - pending, patented or abandoned)
(application serial no.)	(filing date)	(status - pending, patented or abandoned)

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

(provisional application no.)	(filing date)

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

David V. Trask, Reg. No. 22,012	William S. Britt, Reg. No. 20,969	Thomas J. Rossa, Reg. No. 26,799
Laurence B. Bond, Reg. No. 30,549	Joseph A. Walkowski, Reg. No. 28,765	James R. Duzan, Reg. No. 28,393
Allen C. Turner, Reg. No. 33,041	Kent S. Burningham, Reg. No. 30,453	Edgar R. Cataxinos, Reg. No. 39,931
Stephen R. Christian, Reg. No. 32,687	Brick G. Power, Reg. No. 38,581	Kenneth B. Ludwig, Reg. No. 42,814
Paul C. Oestreich, Reg. No. 44,983	Devin R. Jensen, Reg. No. 44,805	Eleanor V. Goodall, Reg. No. 35,162
Kenneth C. Booth, Reg. No. 42,342	Samuel E. Webb, Reg. No. 44,394	David L. Stott, Reg. No. 43,937
Kerry D. Tweet, Reg. No. P-45,959	Michael L. Lynch, Reg. No. 30,871	Lia M. Pappas, Reg. No. 34,095

Address all correspondence to: Brick G. Power, telephone no. (801) 532-1922.
TRASK, BRITT & ROSSA
P.O. BOX 2550
Salt Lake City, Utah 84110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first joint inventor: John Whitman
Inventor's signature _____ Date 3-31-00
Residence: Boise, Idaho
Citizenship: U.S.A.
Post Office Address: 5546 South Boradwing Way, Boise, Idaho 83716

DECLARATION FOR PATENT APPLICATION
(continuation page)

Invention title: SPIN COATING FOR MAXIMUM FILL CHARACTERISTIC YIELDING A PLANARIZED THIN FILM SURFACE

Inventor name(s) appearing on first declaration page: John Whitman

☒ Additional original, first and joint inventor(s):

Full name of second joint inventor: John Davlin
Inventor's signature _______________ Date 31 March 2000
Residence: Nampa, Idaho
Citizenship: U.S.A.
Post Office Address: 5814 East Oak Street, Nampa, Idaho 83687

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Whitman et al.	**Examiner:**	Unknown
Serial No.:	Not yet assigned	**Group Art Unit:**	Unknown
Filed:		**Attorney Docket No.:**	4294US (98-1208)
Title:	SPIN COATING FOR MAXIMUM FILL CHARACTERISTIC YIELDING A PLANARIZED THIN FILM SURFACE		

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE UNDER 37 CFR § 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

MICRON TECHNOLOGY, INC , assignee of the entire right, title and interest by assignment from the inventor(s) in the above-identified application, hereby appoints the following attorneys and agents:

David V Trask, Reg. No. 22,012	William S. Britt, Reg. No. 20,969	Thomas J. Rossa, Reg. No. 26,799
Laurence B. Bond, Reg. No. 30,549	Joseph A. Walkowski, Reg. No. 28,765	James R. Duzan, Reg. No. 28,393
Allen C. Turner, Reg. No. 33,041	Kent S. Burningham, Reg. No. 30,453	Edgar R. Cataxinos, Reg. No. 39,931
Stephen R Christian, Reg No. 32,687	Brick G. Power, Reg. No. 38,581	Kenneth B. Ludwig, Reg. No. 42,814
Paul C Oestreich, Reg. No. 44,983	Devin R. Jensen, Reg. No. 44,805	David L. Stott, Reg. No 43,937
Kenneth C Booth, Reg. No. 42,342	Samuel E. Webb, Reg. No. 44,394	Kerry D. Tweet, Reg. No. P-45,959
Eleanor V Goodall, Reg. No. 35,162	Michael L. Lynch, Reg. No. 30,871	Lia M. Pappas, Reg. No. 34,095

as its attorneys with full power of substitution to prosecute this application and all applications claiming filing date priority therefrom and to transact all business in the U.S. Patent and Trademark Office in connection therewith.

The above-identified assignee hereby elects, pursuant to 37 C.F.R. § 3.71, to conduct the prosecution of the above-identified patent application to the exclusion of the inventor(s).

A chain of title from the inventor(s) of the above-identified patent application to the above-identified assignee is shown:

[] In an assignment recorded in the U.S. Patent and Trademark Office at Reel , Frame .

[X] In an assignment filed herewith for recordation, a true copy of which is attached hereto.

The undersigned has reviewed the above-identified assignment and, to the best of his knowledge and belief, title is in the above-identified assignee.

The undersigned further avers that he is empowered to make and sign the foregoing certification on behalf of the above-identified assignee, and to take the action set forth herein on its behalf.

Please direct all communications regarding the above-identified application to:

Brick G. Power,
TRASK, BRITT & ROSSA
P.O. Box 2550
Salt Lake City, UT 84110
Tele: (801) 532-1922
Fax: (801) 531-9168

Respectfully Submitted,

MICRON TECHNOLOGY, INC.

Date: 3-31-00

By: _____
Michael L. Lynch, Esq.
Reg. No. 30,871
Chief Patent Counsel,
MICRON TECHNOLOGY, INC.